International J. of Engg. Research & Indu. Appls. (IJERIA).
ISSN 0974-1518, Vol.6, No. III (August 2013), pp 107-118

LOW POWER ARCHITECTURE FOR RECONFIGURABLE FIR FILTER FOR SDR

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Abstract

PSM architecture synthesizes multiplier blocks with low hardware requirement suitable for implementation as part of full parallel finite impulse response (FIR) filters is presented in this paper. FIR digital filters are widely used in DSP by the virtue of its stability, linear phase, fewer finite precision error and efficient implementation. In this paper, new reconfigurable architectures of low complexity FIR filters are proposed, namely programmable shifts method. The Methods can be modified by replacing the adder architecture by using carry save adder instead of normal adder architecture. The proposed architectures offer 12% of area and power reductions and compared to the best existing reconfigurable FIR filter implementations in the literature and the proposed architectures have been implemented and tested on Spartan-3 xc3s200-5pq208 field-programmable gate array (FPGA) and synthesized

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Keywords : Channelizer, FIR filter, high level synthesis, CSA, reconfigurability